LISTING OF THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

WHAT IS CLAIMED IS:

1. (Currently Amended) 1. A method of forming a silicon-oxide-nitride–oxide-silicon (SONOS) type non-volatile memory device, comprising:

forming a plurality of first gates on a semiconductor substrate;

forming a plurality of charge storage spacers on a lower sidewall of the plurality of first gates so that an upper sidewall of a given first gate is exposed by a given charge storage spacer ~~is on a sidewall of a given first gate~~; and

forming a plurality of second gates to be self-aligned to the plurality of charge storage spacers at the side of the plurality of first gates so that a given charge second gate covers the exposed upper sidewall of the given first gate and the given storage spacer ~~on the plurality of first gates so that a given second gate is on a sidewall of a given first gate and covers a given charge storage spacer~~.

2. (Original) The method of claim 1, further comprising, prior to forming the plurality of first gates:

forming a device isolating layer defining an active region in a given region of the semiconductor substrate prior to forming the plurality of first gates; and

forming a gate insulating layer on the active region prior to forming the plurality of first gates.

3. (Original) The method of claim 2, wherein

forming the device isolating layer includes forming the device isolating layer in two dimensions along columns and rows, and

forming the plurality of first gates includes forming at least two first gates in parallel on the device isolating layers and disposed along one direction.

4. (Original) The method of claim 2, wherein forming the gate insulating layer includes forming the gate insulating layer by thermal oxidation.

5. (Currently Amended) The method of claim 1, further comprising:

forming a first insulating layer on sidewalls of the given first gate prior to forming the plurality of charge storage spacers.

6. (Currently Amended) The method of claim 1, wherein forming the plurality of charge storage spacers includes:

forming a charge storage layer on the semiconductor substrate and plurality of first gates; and

anisotropically etching the charge storage layer to form the plurality of charge storage spacers, wherein the ~~a~~ given charge storage spacer has a top surface that is lower in relation to a top surface of the ~~a~~ given first gate.

7. (Original) The method of claim 6, wherein anisotropically etching uses an etch recipe that has an etch selectivity with respect to silicon oxide and silicon.

8. (Original) The method of claim 2, further comprising, prior to forming the plurality of second gates:

forming a mask pattern covering an adjoining two first gates and a region between the adjoining first gates;

forming a first impurity region in an active region between the mask patterns with a first ion implantation process using the mask pattern as a mask;

removing any charge storage spacers that are disposed on the first impurity region; and

removing the mask pattern, wherein the active region is confined by the device isolating layers.

9. (Original) The method of claim 8, wherein removing the charge storage spacers includes using an etch recipe that has etch selectivity with respect to silicon oxide and silicon.

10. (Original) The method of claim 8, further comprising:

forming a mask pattern screening the first impurity region;

forming a second impurity region in the active region with a second ion implantation process using the mask pattern as an ion implantation mask;

removing the mask pattern; and

removing any second gates disposed on the first impurity region.

11. (Original) The method of claim 1, further comprising:

forming a second insulating layer to cover the semiconductor substrate and plurality of charge storage spacers, prior to forming the plurality of second gates.

12. (Original) The method of claim 1, wherein forming the plurality of second gates include:

forming a second gate conductive layer on the semiconductor substrate and plurality of charge storage spacers; and

anisotropically etching the second gate conductive layer with an etch recipe that has an etch selectivity with respect to silicon oxide and silicon.

13. (Original) The method of claim 1, further comprising:

forming a source region with an ion implantation process that uses a second gate and a first gate as a mask.

14. (Original) The method of claim 1, further comprising:

forming an interlayer insulating layer on the semiconductor substrate and plurality of second gates;

patterning the interlayer insulating layer to form an opening that exposes top surfaces of the first gates and second gates;

forming a conductive layer filling the opening; and

patterning the conductive layer.

15. (Withdrawn) A silicon-oxide-nitride–oxide-silicon (SONOS) type nonvolatile memory device, comprising:

a plurality of first gates disposed on a given region of a semiconductor substrate;

a plurality of charge storage spacers disposed on the plurality of first gates so that a given charge storage spacer is on a sidewall of a given first gate; and

a plurality of second gates disposed on the plurality of first gates so that a given second gate is on a sidewall of a given first gate and covers a given charge storage spacer.

16. (Withdrawn) The device of claim 15, further comprising:

a plurality of device isolating layers defining an active region disposed in a given region of the semiconductor substrate, wherein the device isolating layers are two-dimensionally disposed along columns and rows.

17. (Withdrawn) The device of claim 16, wherein

the plurality of first gates cross over the plurality of device isolating layers and are parallel to each other, and

a given pair of first gates are disposed on each of the device isolating layers.

18. (Withdrawn) The device of claim 17, wherein

the charge storage spacers are disposed on internal sidewalls of an adjoining two first gates, and

each first gate of the adjoining two first gates crosses over a different device isolating layer.

19. (Withdrawn) The device of claim 18, further comprising:

an impurity region disposed between a given pair of charge storage spacers that are disposed on the internal sidewalls of the adjoining two first gates, wherein the impurity region represents a common source line of adjoining cell transistors.

20. (Withdrawn) The device of claim 17, further comprising:

an impurity region disposed between a given pair of first gates crossing over the same device isolating layer, wherein the impurity region is divided by the device isolating layer.

21. (Withdrawn) The device of claim 20, further comprising:

a plurality of insulating spacers disposed adjacent to the impurity region, each insulating spacer disposed on another sidewall of a given first gate opposite to the sidewall on which a given charge storage spacer is disposed.

22. (Withdrawn) The device of claim 20, further comprising:

a material pattern disposed adjacent to the impurity region and on another sidewall of a given first gate opposite to the sidewall on which a given charge storage spacer is disposed, wherein the material pattern is formed of an material substantially identical to a material of the second gate.

23. (Withdrawn) The device of claim 15, wherein the first gates and second gates are composed of at least one material selected from a group comprising polysilicon, silicide and metal.

24. (Withdrawn) The device of claim 15, wherein the plurality of charge storage spacers are formed of silicon nitride or silicon oxynitride.

25. (Withdrawn) The device of claim 16, wherein each of the charge storage spacers includes a sidewall that is formed on a device isolating layer to isolate a charge storage spacer

from another charge storage spacer.

26. (Withdrawn) The device of claim 15, further comprising:

a gate insulating layer interposed between the first gates, second gates, charge storage spacers and semiconductor substrate;

a first insulating layer interposed between the plurality of first gates and the plurality of charge storage spacers;

a second insulating layer interposed between the plurality of charge storage spacers and the plurality of second gates; and

a connector connecting the first gates and second gates, wherein the gate insulating layer and the first insulating layer are composed of silicon oxide.